ESD Detection Circuit controlling to using ESD Clamp Circuit with adjustable holding voltage and PMOS-Based Power

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Abstract - A new power-rail ESD clamp circuit designed with PMOS as main ESD clamp device has been proposed and verified in a 65nm 1.2V CMOS process. The new proposed design with adjustable holding voltage controlled by the ESD detection circuit has better immunity against mis-trigger or transient-induced latch-on event. The layout area and the standby leakage current of this new proposed design are much superior to that of traditional RC-based power-rail ESD clamp circuit with NMOS as main ESD clamp device.

Index Terms— transmission line pulsing ,RC-based power-rail ESD clamp circuit ,CMOS process,ESD clamp device,PMOS transistor,DC I-V Measurement

I. Introduction

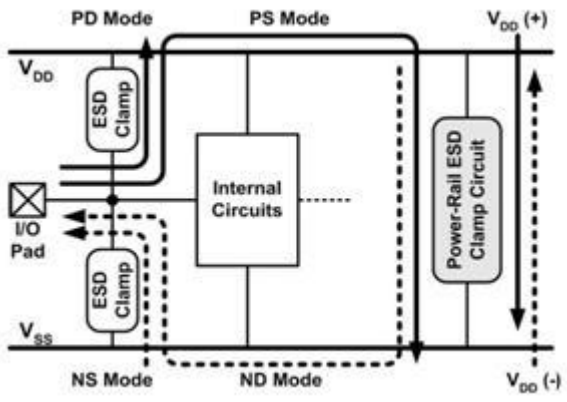
In advanced nanoscale CMOS process, electrostatic discharge (ESD) protection has become the major concern of reliability for integrated circuits (ICs). The nanoscale device with thinner gate oxide and shallower diffusion junction depth seriously degrades the ESD robustness of ICs and raises the difficulty of ESD protection design for ICs implemented in nanoscale CMOS technology[1].Therefore,an efficient ESD protection elementis highly required by IC industry. To achieve whole-chip ESD protection,the power-rail ESD clamp circuit is a vital basis, as shown in Fig. 1 [2]. In Fig.1, the power-rail ESD clamp circuit can protect the internal circuits with efficient discharging path under various ESD stress conditions.

The ESD clamp device drawn in the layout style of big field-effect transistor (BigFET) had revealed excellent ESD protection performance in advanced nanoscale CMOS ICs[3]-[6].For the ESD-transient detection circuit, there are two design skills, the RC-delay [3]-[4] and the capacitance-coupling designs [5]-[6], to effectively trigger the BigFET transistor under ESD stress condition. The traditional RC-based power-rail ESD clamp circuit is shown in Fig. 2. The RC time constant is generally designed large enough about several hundreds nanosecond to keep the ESD clamp device at "ON" state under ESD stress condition. However, the extended RC time constant of the ESD-transient detection circuit suffers not only the larger layout area but also the mis-trigger of the ESD clamp circuit under fast-power-on or "hot-plug" applications [3].

Figure 1: Whole-chip ESD protection design with power-rail ESD clamp circuit under different ESD stress conditions.

Besides, low standby leakage of the ESD clamp circuit is highly demanded by the hand-held, portable,and battery powered products. In advanced CMOS technology, the leakage current of NMOS was often larger than that of PMOS in the same device dimension. Therefore, PMOS is suggested to be used as ESD clamp device [7].

In this work, the parasitic capacitance of the ESD clamp PMOS transistor drawn in BigFET layout style is used as a part of ESD-transient detection circuit.This new design has been verified in a 65nm 1.2V CMOS technology. From the measured results, the proposed power-rail ESD clamp circuit has features of area efficiency, low leakage current, and high immunity against mis-trigger.



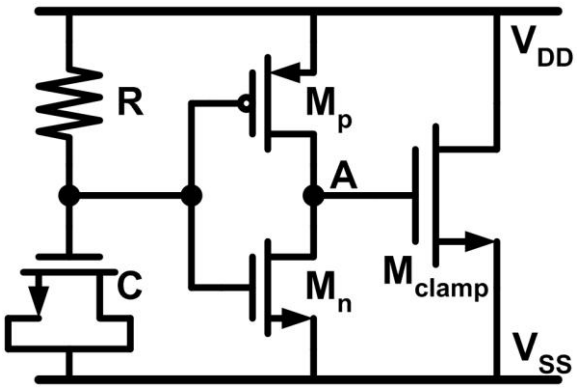


Figure 2: Traditional *RC*-based power-rail ESD clamp circuit.

II. New Power-Rail ESD Clamp Circuit

A. New ESD-Transient Detection Circuit

The new proposed power-rail ESD clamp circuit is illustrated in Fig. 3. The ESD-transient detection circuit consists of two transistors (M_n and M_p), two resistors (R_n and R_p), and diode string. The PMOS transistor drawn in BigFET layout style (M_{clamp}) is used as ESD clamp device. The gate terminal of M_{clamp} is linked to the output of the ESD-transient detection circuit, which can command M_{clamp} at "ON" or "OFF" state.

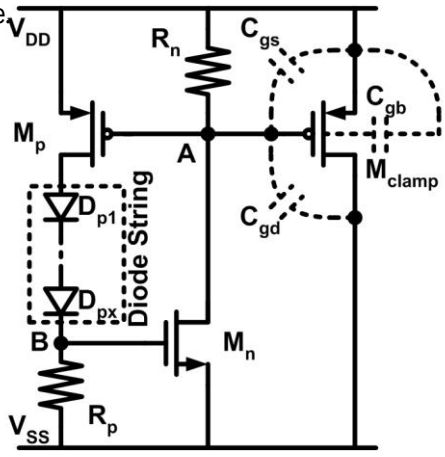


Figure 3: Proposed power-rail ESD clamp circuit with diode string in the ESD-transient detection circuit.

In Fig. 3, the diode string in ESD-transient detection circuit is used to adjust the holding voltage to overcome the transient-induced latch-on issue. In this work,the ESD-transient detection circuits with zero,one, and two diodes were investigated in silicon chip. The measured results reveal that the holding voltage of the power-rail ESD clamp circuit can be adjusted by modifying the number of the diodes in the ESD-transient detection circuit. In addition, the new proposed power-rail ESD clamp circuit can be totally turned off after power-on transition because the nodes A and B are kept at V_{DD} and V_{SS} through the resistors Rn and Rp respectively.

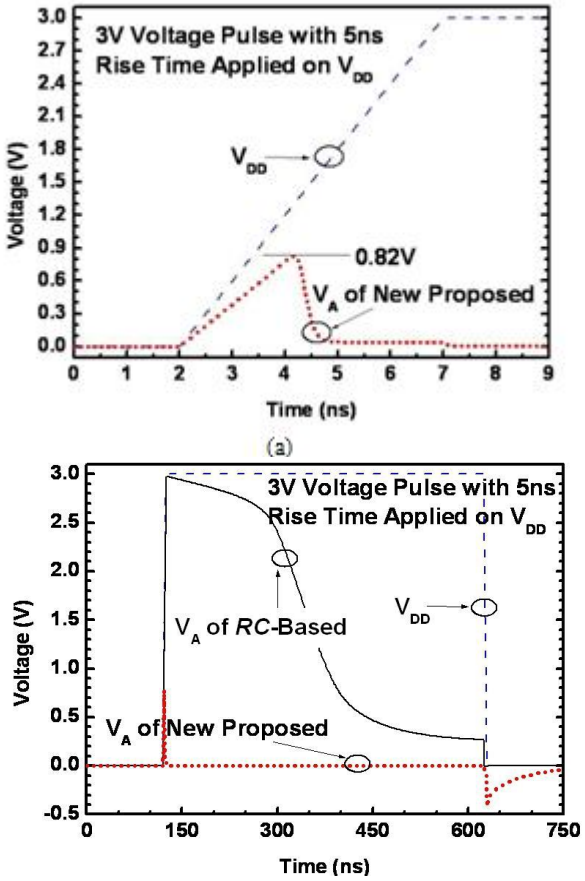
B. Operation Principle under ESD Stress

The ESD clamp PMOS transistor is drawn in BigFET without silicide blocking.Large C_{gd}, C_{gs} and C_{gb} parasitic capacitances essentially exist in the ESD clamp PMOS transistor. These parasitic capacitances and the resistor R_n can be used to realize capacitance coupling mechanism in the power-rail ESD clamp circuit. In Fig. 3, the gain (G) of the coupling effect caused by C_{gd}, C_{gs}, C_{gb}, and R_n during the positive VDD-to-VSS ESD stress condition can be expressed as

$$G = \frac{V_A}{V_{DD}} = \left| \frac{\frac{1}{j\omega C_{gd}}}{\frac{1}{j\omega C_{gd}} + \left(\frac{1}{R_n} + j\omega(C_{gs} + C_{gb})\right)^{-1}} \right|$$

According to the device sizes used in this work, the gain is 0.64 with C_{gd}≒C_{gs}=0.44pF,C_{gb}=0.35pF,R_n=40kΩ and signal frequency of 50MHz derived from 5ns fast-rising edge of the ESD voltage pulse.A 3V voltage pulse with a rise time of 5ns is applied to the V_{DD} node while the V_{SS} node was grounded to simulate the fast-rising edge of the HBM ESD event, as shown in Fig. 4(a). The coupling voltage at node A (V_A) of the proposed circuit is exactly equal to 0.64V_{DD} before the ESD-transient detection circuit is turned on. When the voltage difference between V_{DD} and V_A is getting larger, the sub-threshold current of M_p can produce enough voltage difference on R_p to further turn on M_n, the V_A will be quickly pulled down to the ground level to trigger on the ESD clamp PMOS transistor. In Fig. 4(b), the pulled-down V_A of the proposed circuit can be kept at low voltage level during whole voltage pulse duration. However, the V_A in the traditional RC-based power-rail ESD clamp circuit, as shown in Fig. 2, is elevated to the voltage level higher than the NMOS threshold voltage of ~0.58V for only the first period of ~300ns. The design parameters, including the device sizes of each

transistor and resistor, are listed in Table 1.



(b)

Figure 4: The simulation results of the voltage transient on V_{DD} and node A under a 3V voltage pulse with a rise time of 5ns.
(a) The voltage waveforms in the period of rising transition, and
(b) The voltage waveforms during the whole voltage pulse of 500ns.

Table 1: Device Sizes of the Power-Rail ESD Clamp Circuits

Design Parameters	*RC*-Based ESD Clamp Circuit	New Proposed ESD Clamp Circuit
Capacitor	64 μm / 2 μm (W/L)	none
Resistor (Ω)	R = 113k	R_n = 40k ; R_p = 20k
PMOS Transistor (M_p)	184 μm / 60 nm	24 μm / 60 nm
NMOS Transistor (M_n)	36 μm / 60 nm	12 μm / 60 nm
ESD Clamp Transistor (M_{clamp})	2000 μm / 100 nm (NMOS)	2000 μm / 100 nm (PMOS)
Diode (D_o)	none	0.057 μm²

For the latch-on issue, the holding voltage (V_h) of the proposed power-rail ESD clamp circuit can be calculated as

$$V_h = V_{ds(M_p)} + nV_{ON(Diode)} + V_{gs(M_n)}$$

$$= V_{ds(M_p)}\Big|_{I_{ds}=\frac{V_{THN}}{R_p}} + nV_{ON(Diode)} + V_{THN}$$

$$\approx nV_{ON(Diode)} + V_{THN}$$

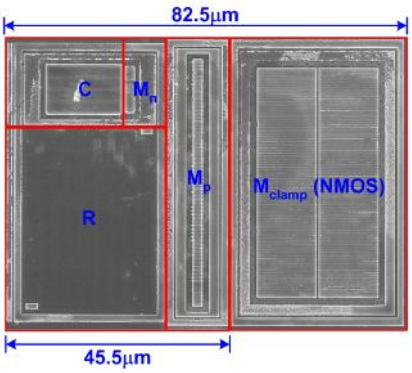
where n and V_{ON} are the number and the turn-on voltage of the diode, respectively. Based on the simulation results, the V_h can be represented as the summation of V_{ON} (0.71V) and V_{THN} (0.58V) due to minor V_{ds} (~ few milli-volt).

III. Experimental Results

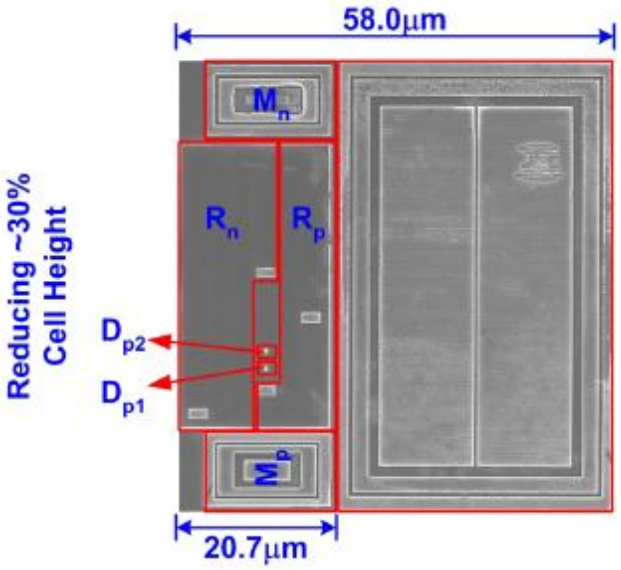
The test chip to verify the proposed power-rail ESD clamp circuit has been fabricated in a 65nm 1.2V CMOS process. As shown in Figs. 5(a) and (b), the layout area of the proposed ESD-transient detection circuit is reduced by 54.5% from that of traditional RC-based one.

A. DC I-V Measurement

The leakage currents of the power-rail ESD clamp circuits at 1.2V normal circuit operation voltage are measured in Fig. 6.The leakage current of the traditional RC-based power-rail ESD clamp circuit is 86.9nA at room temperature. However, the proposed power-rail ESD clamp circuits with different numbers of diodes have the leakage currents in the range of 15nA to 17nA. The leakage current of the proposed power-rail ESD clamp circuit is extremely reduced by 80.4%. Therefore, the proposed power-rail ESD clamp circuit with lower leakage current is more adequate for the portable products, which highly require low standby leakage current.



(a)



(b)

Figure 5: Chip microphotographs of
(a) The traditional *RC*-based power-rail ESD clamp circuit
(b) The proposed power-rail ESD clamp circuit with two diodes in its ESD-transient detection circuit

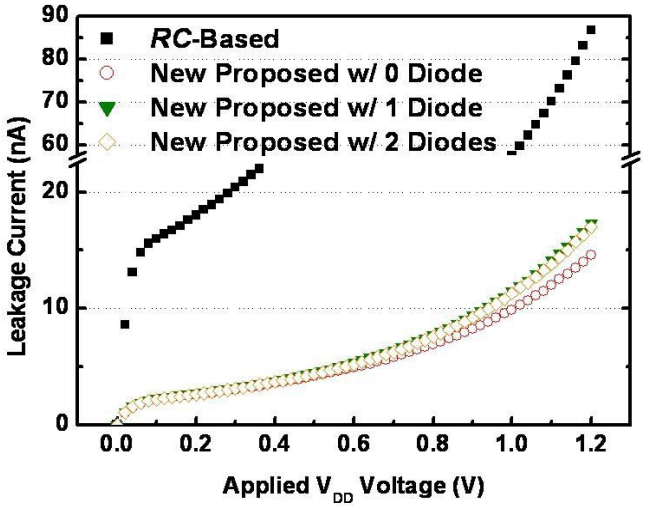


Figure 6: The measured DC I-V curves of the traditional *RC*-based and the proposed power-rail ESD clamp circuits at room temperature

B. TLP Measurement

The transmission line pulsing (TLP) generator with a pulse width of 100ns and a rise time of ~2ns is used to measure the fabricated power-rail ESD clamp circuits [8]. As shown in Fig. 7(a), there are no differences among the curves higher than 3.5V because the device sizes of M_{clamp} in all proposed power-rail ESD clamp circuits are the same. The second breakdown currents (It_2) of the traditional RC-based and the proposed power-rail ESD clamp circuits are 5.44A and 5.01A, respectively.

The holding voltages of the proposed ESD-transient detection circuits with zero, one, and two diodes are 0.56V, 1.25V, and 2.12V, respectively, as shown in Fig. 7(b). They are very close to the theoretical ones of 0.58V, 1.29V, and 2.00V calculated from (2). The ESD-transient detection circuit with the adjustable holding voltage has been successfully verified, which can be safely applied to protect any internal circuit from the transient-induced latch-on event.

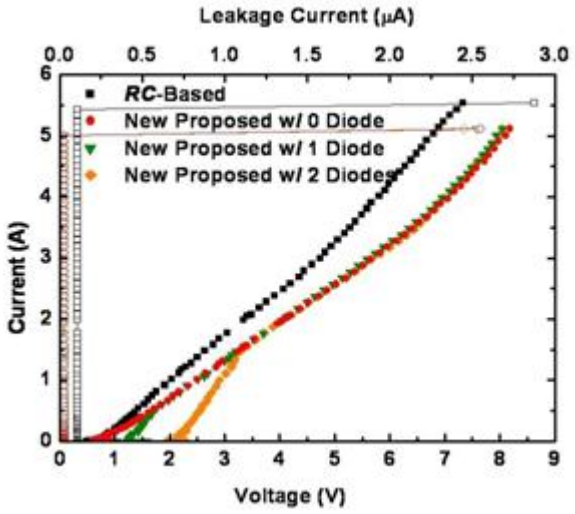
Table 2 shows the HBM and MM ESD robustness of these four power-rail ESD clamp circuits. The HBM ESD robustness of all power-rail ESD clamp circuits are over 8kV. The MM ESD robustness of the traditional RC-based and the proposed power-rail ESD clamp circuits are 450V and 350V, respectively.

Power-Rail ESD Clamp Circuits	It_2 (A)	HBM Level (kV)	MM Level (V)
Traditional *RC*-Based	5.44	> 8	450
New Proposed with 0 Diode	5.01	> 8	350
New Proposed with 1 Diode	5.01	> 8	350
New Proposed with 2 Diodes	5.01	> 8	350

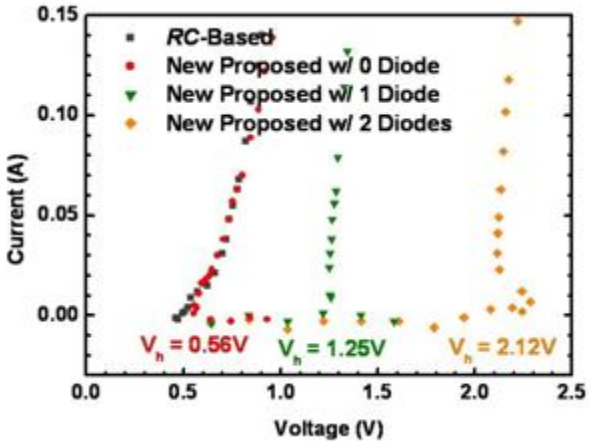
Table 2: Measured Results of Second Breakdown Current and ESD Levels of Four Power-Rail ESD Clamp Circuits

C. Turn-On Verification

For the turn-on verification, a 3V voltage pulse with 5ns rise time to simulate the rising transition of HBM ESD event is applied to the V_{DD} power line with the grounded V_{SS}. In Fig.8(a), the voltage waveform of the traditional RC-based design rises as the time increases. On the contrary, the voltage waveforms of the proposed designs with different numbers of diodes are clamped to the specific voltage levels during the whole pulse duration due to the positive feedback mechanism in the proposed ESD-transient detection.



(a)

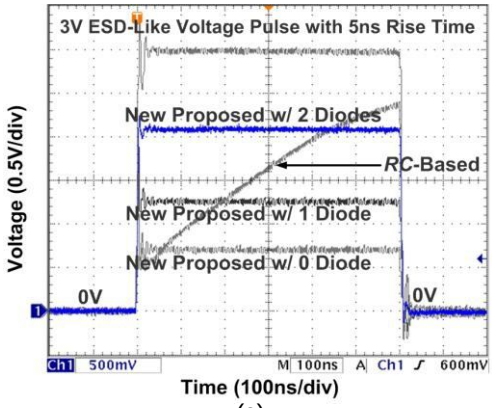


(b)

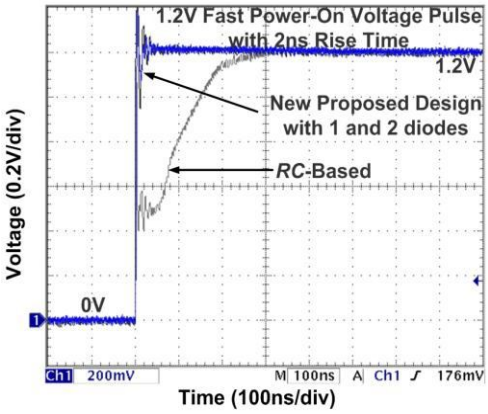
Figure 7: TLP measured I-V curves of (a) the power-rail ESD clamp circuits and (b) the zoomed-in illustration for the holding voltages.

circuit.Some previous studies [3]-[4] had shown that the ESD-transient detection circuits with the RC-based design and feedback mechanism were easily mis-triggered into the latch-on state [9] under the fast power-on condition. For the fast power-on condition, a voltage pulse with 1.2V and 2ns rise time is applied in this work. As shown in Fig. 8(b), the voltage waveforms of the proposed power-rail ESD clamp circuits with one and two diodes are not degraded.

The proposed power-rail ESD clamp circuits have high immunity against mis-trigger due to adjustable holding voltage. On the contrary, the RC-based power-rail ESD clamp circuit dramatically suffers the mis-trigger, which spends about 300ns to return back the normal circuit operation voltage level of 1.2V, as shown in Fig. 8(b).In addition, the turn-on verification with the power line noise at normal circuit operation is another useful justification for the latch-on concerns. The transient noise with 3V voltage level and a rise time of 5ns is purposely added to V_{DD}.



(a)



(b)

Figure 8: The voltage waveforms monitored on the power-rail ESD clamp circuits under

(a) ESD-transient-like condition and

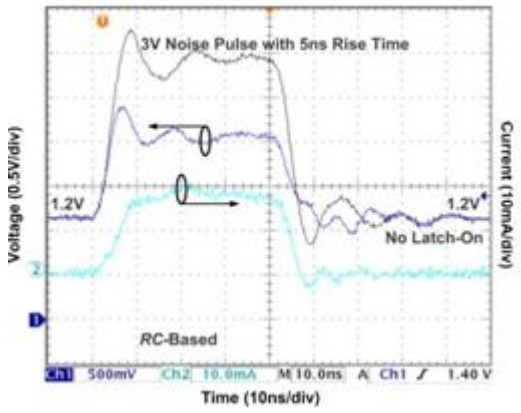
(b) Fast-power-on condition

power line with 1.2V operation voltage. As shown in Figs. 9(a) to (c), the new proposed ESD-transient detection circuit with zero diode is the only circuit to suffer the latch-on issue because its holding voltage is much lower than the 1.2V operation voltage.

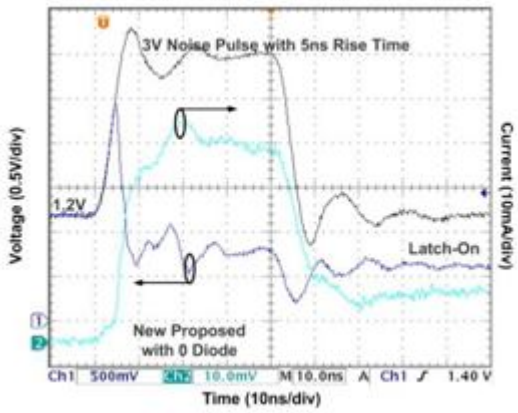
However, the holding voltage of the new proposed ESD-transient detection circuit can be adjusted by adding the diodes.Therefore, the ESD-transient detection circuits with positive feedback mechanism and the adjustable holding voltage can be free to latch-on issue. Since the feedback mechanism was not used in the traditional RC-based power-rail ESD clamp circuit, the latch-on event was not occurred

in such a measurement.

Based on the design concept discussed above, the power-rail ESD clamp circuit realized with NMOS as main ESD clamp device was also verified in [10]. However, PMOS based power-rail ESD clamp circuit has further lower leakage than that work with NMOS.



(a)



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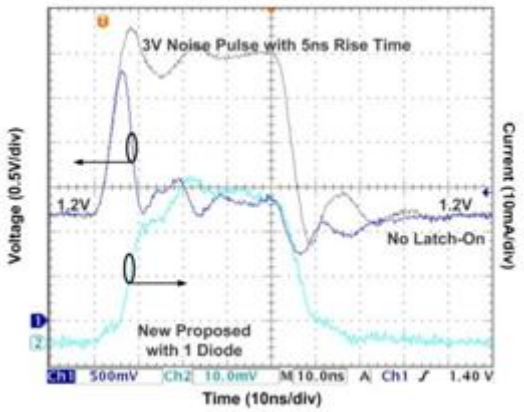

(c)

Figure 9: The measured voltage and current waveforms of powerrail ESD clamp circuit, realized with

(a) the traditional *RC*-based ESD-transient detection circuit,

(b) The proposed ESD-transient detection circuit with no diode,

(c) The proposed ESD-transient detection circuit with one diode, under transient noise condition with 3V overshooting on1.2V and V_{DD}.

IV. Conclusion

New power-rail ESD clamp circuit with adjustable holding voltage has been successfully verified in a 65nm 1.2V CMOS technology. The proposed ESD-transient detection circuit adopts the capacitance-coupling mechanism to command the ESD clamp PMOS transistor. From the measured results, the proposed design has excellent immunity against mis trigger and latch-on under the fast power-on condition. The proposed ESD-transient detection circuit is also efficient in layout area and standby leakage, which save layout area and leakage current by more than 54.5% and 80.4%, respectively, compared with the traditional RC-based ESD-transient detection circuit.

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